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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/083,042	02/26/2002	Rong-Feng Chang	71795/20592	3126

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EXAMINER	
PATEL, FAHD	

ART UNIT	PAPER NUMBER
2194	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/083,042	CHANG ET AL.	
	Examiner	Art Unit	
	Fahd Patel	2194	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 February 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/26/02, 4/24/02,* 3/25/05
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-40 are pending in this application.

Claim Rejections - 35 USC § 101

2. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

3. Claims 21-40 are directed to method steps which can be practiced mentally in conjunction with pen and paper, therefore they are directed to non-statutory subject matter. Specifically, as claimed, it is uncertain what performs each of the claimed method steps. Moreover, each of the claimed steps, inter alia, providing and connecting can be practiced mentally in conjunction with pen and paper. The claimed steps do not define a machine or computer implemented process (see MPEP § 2106). Therefore, the claimed invention is directed to non-statutory subject matter. It is suggested that the applicant changed the term "method" in the preamble to "computer implemented methods" to overcome this rejection.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1-40 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

a. The following terms lack antecedent basis:

i. "the architecture" (claims 2, 15).

ii. "the header" (claim 15).

b. The following claim language is indefinite:

i. As per claim 1, line 4, it is unclear what the term "managing" means in the context of the invention. Specifically, it is unclear what type of management is occurring, since the general definition of task management refers to an operating system environment whereas this is a chip level hardware environment.

ii. As per claim 2, lines 2-3, it is unclear what "the architecture" refers to (i.e.: the task-based chip-level hardware architecture or the plurality of task modules arranged in a star topology).

iii. As per claim 4, lines 1-2, it is uncertain how the task is a "predefined function". Specifically, if there is any relationship between the task information and the predefined function that is dedicated to the task module.

iv. As per claim 7, it is unclear what potential effect the topology would have on the task module, and thus what it means for it to function "independently".

v. As per claim 8, line 2, it is unclear what is meant by: "by switching task management among a plurality of task modules". Specifically, it is unclear what defines which task modules can have the task management function. It is unclear why the task module would have that management function since it is "performing a predefined task". It is unclear if the architecture *further comprises* a plurality of task modules wherein the task manager performs a switching function by switching among a plurality of said task modules.

vi. As per claim 13, line 2, the word "which" is unclear. It is suggested that the applicant changes this to "said".

vii. As per claim 15, line 2, it is uncertain what is meant by "by including at least one of embedding a task list in the header".

(1) To clarify this sentence, examiner recommends placing a colon after "at least one of".

(2) It appears that "the header refers to "header data" from claim 14, line 2, although this is not a proper reference.

Line 2, it is unclear how the dispatch information can contain a "task list" since the dispatch information is for a specific task, and not a group of tasks. This could possibly relate to a list of subtasks, but that is not mentioned anywhere. Line 3, it is unclear whether the same mapping table is stored in both the task manager and the task module, and if so, what the purpose of the duplicate is.

viii. As per claim 16, line 2, the phrase "core sublayer" is unclear. Specifically, it is unclear if the task module further comprises one or more state machines wherein the state machine interfaces with one or more auxiliary modules.

ix. As per claim 18, lines 2-3, it is unclear structurally how the task managers and modules will be situated within the tree topology in order to provide the proposed communication. Specifically, a tree consists of root and leaf nodes, therefore it is unclear how "a plurality of task modules are provided in communication with a plurality of task managers" within the constraints of a tree topology.

x. As per claim 20, line 2, the term "which" (line 15) is unclear. It is recommended that it be changed to "said".

xi. As per claims 21-22, 24, 27-28, 33, 35-36, 38, 40, they have the same deficiencies as claims 1-2, 4, 7-8, 13, 15-16, 18, 20 respectively.

xii. Claims 22-40 are unclear because they add structural content in their addition to method steps.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the

applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1-5, 7, 8, 12, 13, 16, 17, 21-25, 27, 28, 32, 33, 36, and 37 are rejected under 35 U.S.C. 102(e) as being anticipated by Imanishi et al. (U.S. Patent 6,243,735 B1) hereafter Imanishi.

8. As per claim 1, Imanishi teaches the invention as claimed including a task-based chip-level hardware architecture (abstract, lines 2-4) comprising:

a task manager for managing a task with task information; (101, Fig 1; 201, Fig 2; column 1, lines 47-51; column 3, lines 22-24; column 3, lines 51-55) and

a task module operatively connected to the task manager for performing the task in accordance with the task information (column 2, lines 62-63; 111-115, Fig 1).

9. As per claim 2, Imanishi teaches a plurality of task modules (211-216, Fig 2) that are in operative communication with the task manager (201, Fig 2), wherein the architecture is structured according to a star topology (see figure 1, with the task module contained within the microcontroller).

10. As per claim 3, Imanishi teaches that the task manager is a hub of the start topology (see figure 1, with the task module contained within the microcontroller).

11. As per claim 4, Imanishi teaches that the task is a predefined function dedicated to the task module (column 4, lines 56-62, with the "core" as the task module).

12. As per claim 5, Imanishi teaches that the task module communicates only with the task manager (figure 4, with the "microcontroller" as the task manager and the "core" units as the task modules).

13. As per claim 7, Imanishi teaches that the task module functions independently of a topology in which it is utilized (column 9 lines 10-11, with "data processing systems" as topology).

14. As per claim 8, Imanishi teaches that the task manager performs a switching function by switching task management among a plurality of task modules (column 9, lines 31-39), each of the plurality of task modules performing a predefined task (column 5, lines 28-35; column 9, lines 12-15).

15. As per claim 12, Imanishi teaches an auxiliary module that provides a support function to the task module (figure 1, with the "buffer memory" as the auxiliary module).

16. As per claim 13, Imanishi teaches an auxiliary module that provides a support function to the task module, and which auxiliary module communicates only with the task module (figure 1, with the "buffer memory" as the auxiliary module).

17. As per claim 16, Imanishi teaches that the task module comprises a core sublayer for performing the task, which core sublayer includes one or more state machines and accompanying logic to perform the task (column 2 lines 61-65; column 3, lines 12-22), and interfaces with one or more auxiliary modules (116-118, figure 1).

18. As per claim 17, Imanishi teaches that the task module comprises a message processor that provides a messaging interface between the task manager and the task module. (column 4 lines 48-50, with the "instruction decoder" as the message processor).

19. As per claims 21-25, 27, 28, 32, 33, 36, and 37 see rejections to claims 1-5, 7, 8, 12, 13, 16, and 17 respectively.

Claim Rejections - 35 USC § 103

20. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

21. Claims 6, 9, 14-15, 26, 29, and 34-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Imanishi as applied to claims 1 and 21 above.

22. As per claim 6, Imanishi does not explicitly teach the use of a dedicated port. However, he does teach that the task module communicates only with the task manager, and thus the communication is dedicated (see rejection to claim 5 above). The feature that the task module operatively connects to the task manager via a dedicated port is obvious to one of ordinary skill in the art at the time of the invention because using a dedicated port for dedicated communication is a standard computing practice.

23. As per claim 9, Imanishi does not teach using a 32-bit bus. However, Imanishi teaches that the task information is exchanged between the task manager and the task module via a bus (Figs 1-2).

It would have been obvious to one of ordinary skill in the art at the time of the invention to include a 32-bit bus in Imanishi's system because employing a 32-bit bus in hardware communication is standard practice. Therefore, using a 32-bit bus is an obvious embodiment of Imanishi.

24. As per claim 14, Imanishi does not describe the nature of the task message. However a task message having header data and payload data, which header data includes dispatch information for routing task messages, and which payload data includes packet information associated with packet data on which the task is performed is obvious to one of ordinary skill in the art because the description is identical to that of

a TCP packet. It is common computing knowledge that a TCP packet (as well as many other types of communication messages) contains a header, which includes routing information (port number) and a body that contains the application information. Therefore the task message composition is analogous to that of a TCP packet.

25. As per claim 15, Imanishi teaches storing a mapping table in the task manager, (column 6 lines 38-41).

Imanishi does not teach storing the mapping table in the task module. However, it would have been obvious to one of ordinary skill in the art at the time of the invention to have an extra copy of the mapping table in the task module because copying the mapping table into the task module would improve the throughput of Imanishi's system by having the needed information local to the task module. Therefore it is an obvious improvement to Imanishi.

26. As per claims 26, 29, 34, and 35, see the rejections of claims 6, 9, 14, and 15 above

27. Claims 10-11 and 30-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Imanishi as applied to claims 1 and 21 above, in further view of Weschler et al. (U.S Patent 6,807,181 B1) hereafter Weschler.

28. As per claims 10 and 30, Imanishi does not teach that permission is required for data to be sent. However, Weschler teaches that the task information is transmitted from a sender only when a recipient permits transmission therefrom (column 4 lines 36-43).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Imanishi and Weschler because Weschler's transmission of data only when permission is granted would simplify the control on Imanishi's system.

29. As per claim 11 and 31, Imanishi teaches that when the sender is the task manager, the recipient is the task module, and when the sender is the task module, the recipient is the task manager (column 3 lines 4-6).

30. Claims 18-20 and 38-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Imanishi as applied to claims 1 and 21 above, in further view of Davis et al. (U.S Patent 5,291,611), hereafter Davis.

31. As per claim 18, Imanishi teaches a tree topology (Figs 1-2).

Imanishi does not explicitly teach that a plurality of task modules are provided in communication with a plurality of task managers. However, Davis teaches that a plurality of task modules are provided in communication with a plurality of task

managers (column 3 lines 30-35, with the modular component containing both the task module as the "input gate array" and the task manager as the "DSP chip").

It would have been obvious to one of ordinary skill in the art at the time of the invention to include more than one task manager in Imanishi's system because it would have improved its capability of load balancing the task by having more available resources.

32. As per claim 19, Davis teaches a first task manager and a second task manager that are in direct communication with one another to facilitate completion of the task (column 3 lines 30-53).

33. As per claim 20, Davis teaches a plurality of task modules operatively communicating over respective ports with the task manager, which task manager receives input data and manages processing of the input data into output data by selectively routing input data information in the form of task messages through one or more of the plurality of task modules to generate the output data (column 2 lines 9-20, with the "input gate array" as the task manager and the "DSP" as the task module).

34. As per claims 38-40, see the rejection for claims 18-20 above.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fahd Patel whose telephone number is (571) 272-1044. The examiner can normally be reached on 8:00 am - 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

FHP

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